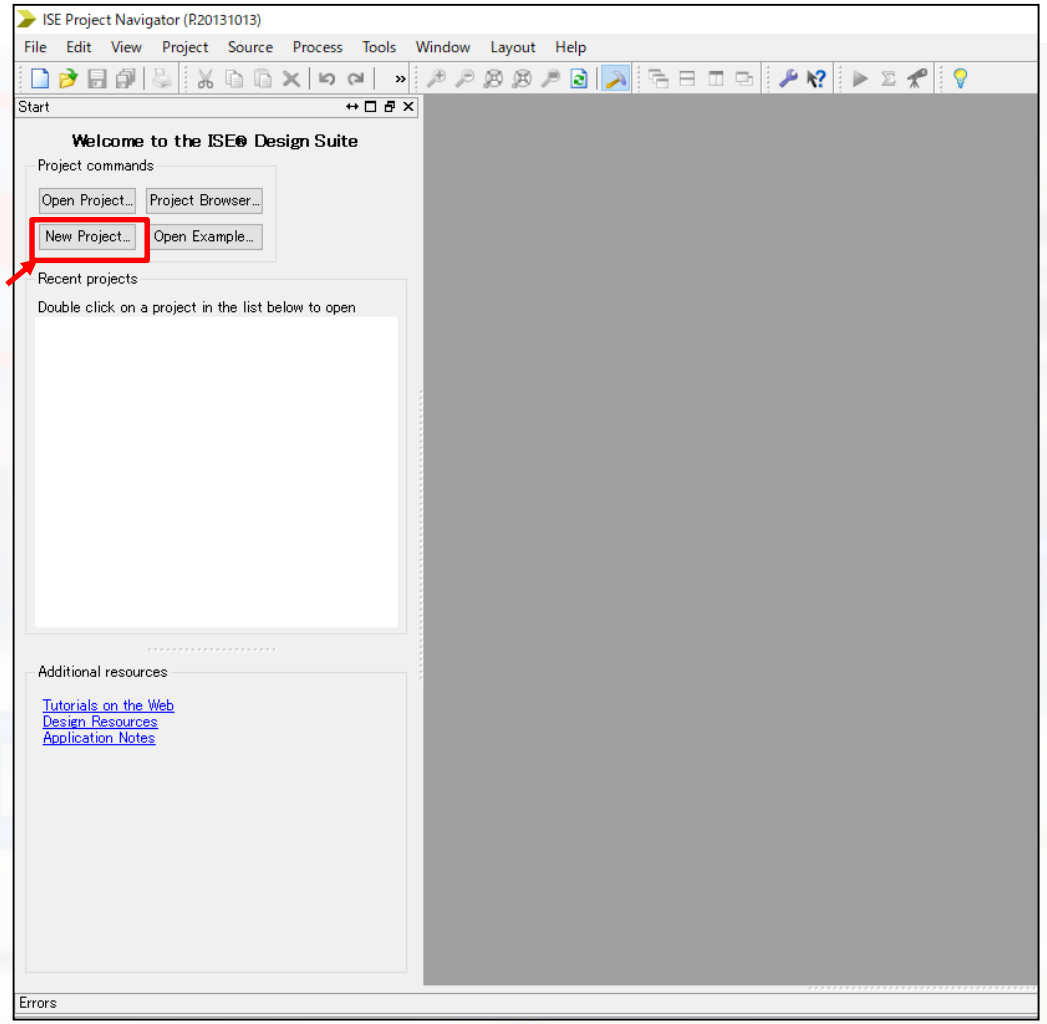
Running Verilog-HDL file - tutorial

LSI Design Contest 2018

Opening ISE Design Suite

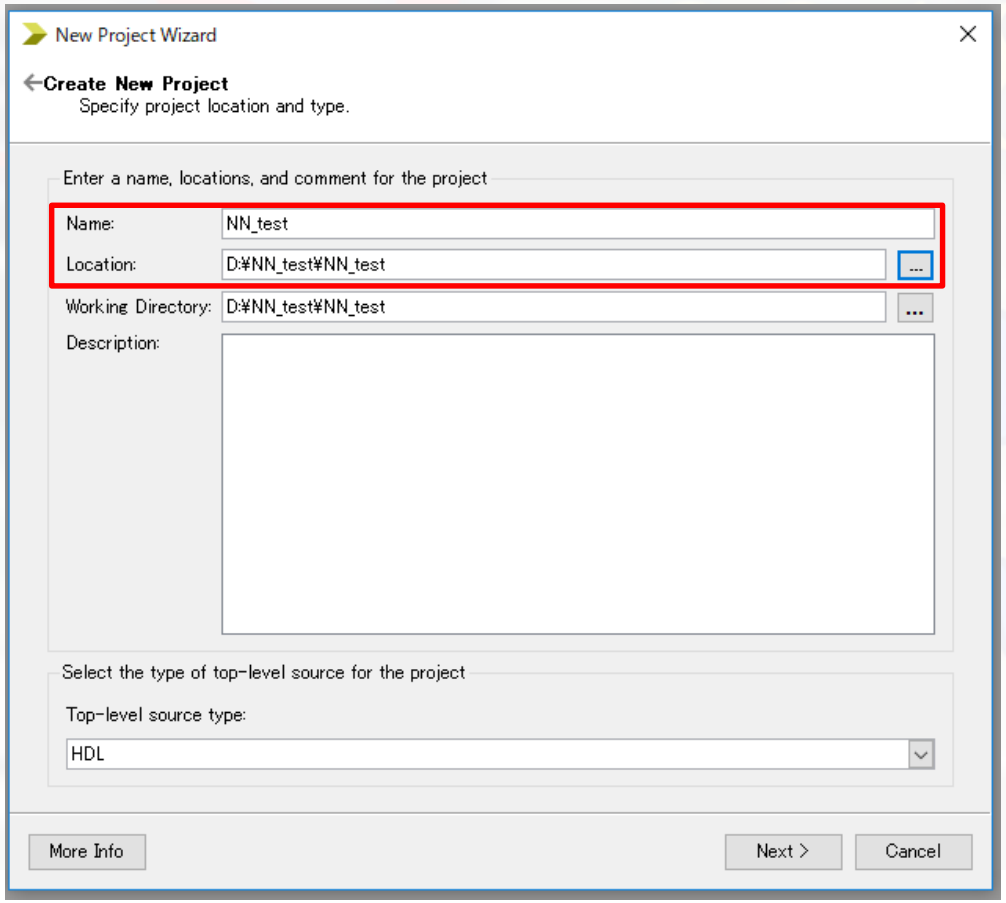
- Open ISE Design Suite
  - Note that the version used here is 14.7

  - Next, click the「New Project…」as shown in the figure.



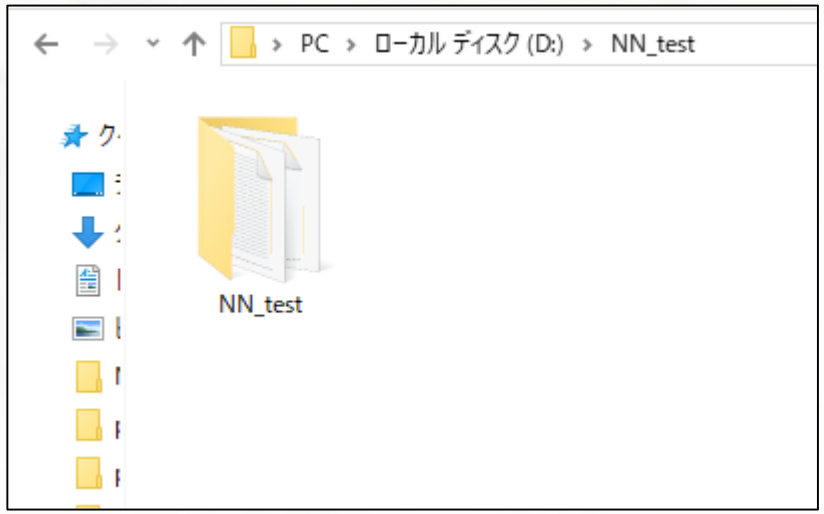
Locating project file

- Assign the location to your selected folder
- Enter the name
  - For example : NN_test
- Click, next, next and finish.

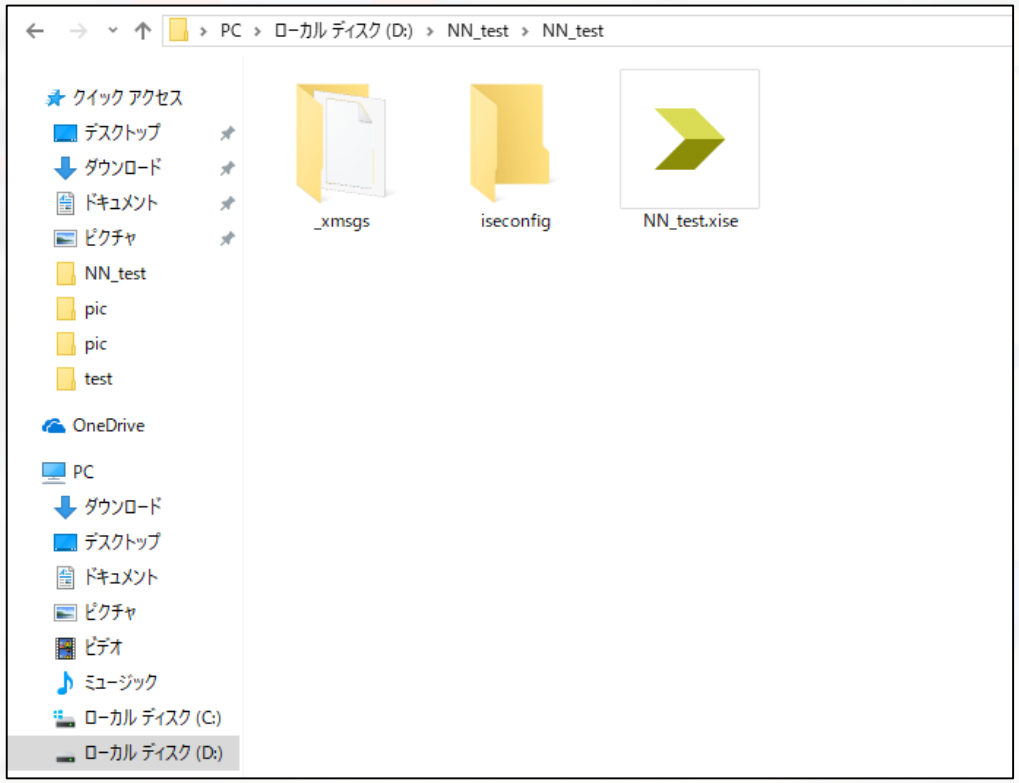


Locating project file

- A new folder will be created in your selected location

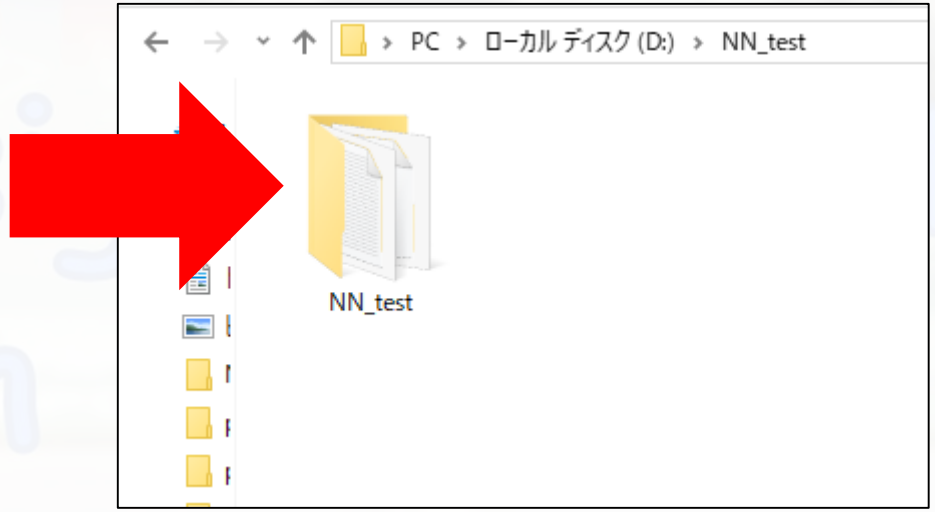


contents



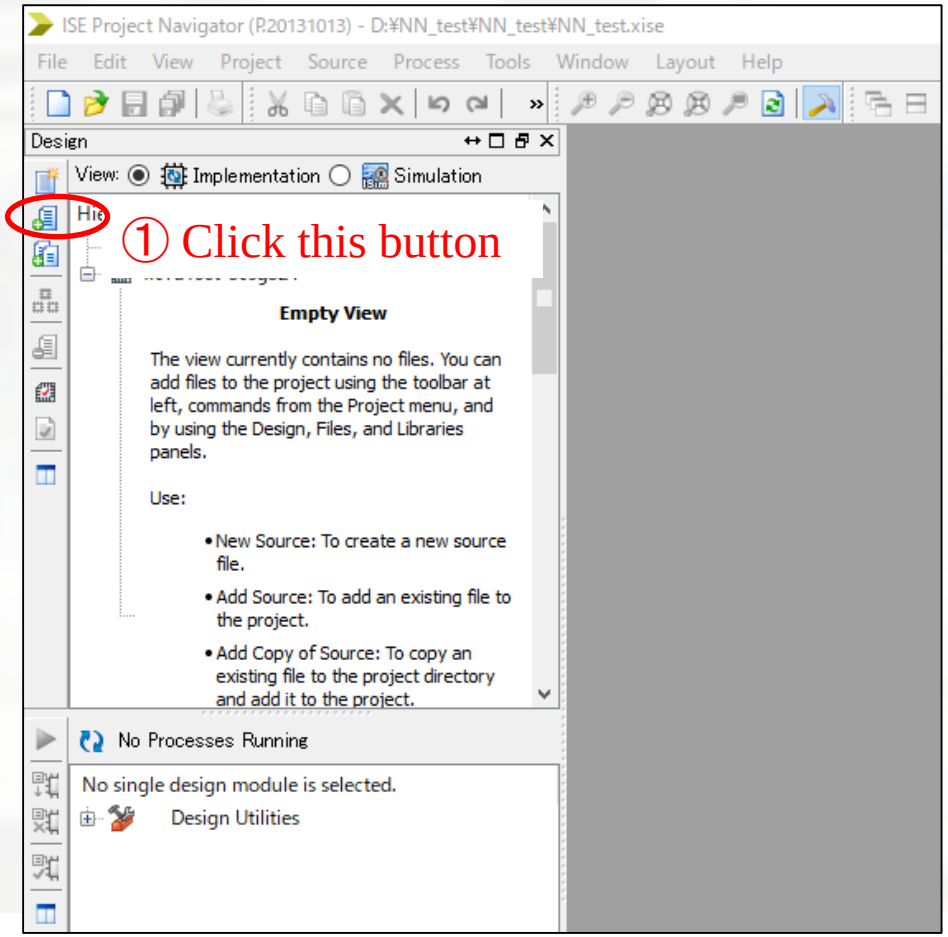
Download Verilog file

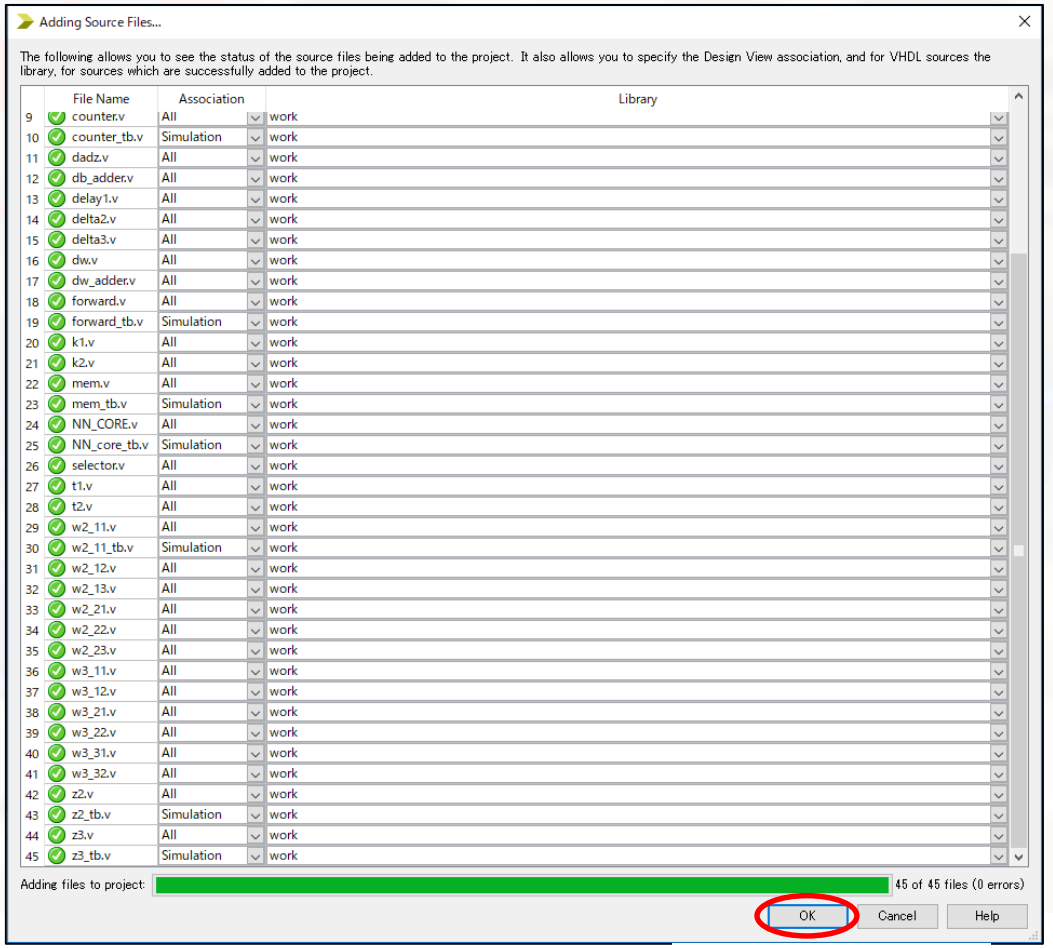
- Download the zip file from LSI design contest HP.
  - Link : http://www.lsi-contest.com/shiyou_4e.html
    - (Verilog file for simulation)
- Extract the file
  - There will be around 45 Verilog file
- Move all the Verilog file into NN_test folder



Add source file

- Click Add source and select all the Verilog file

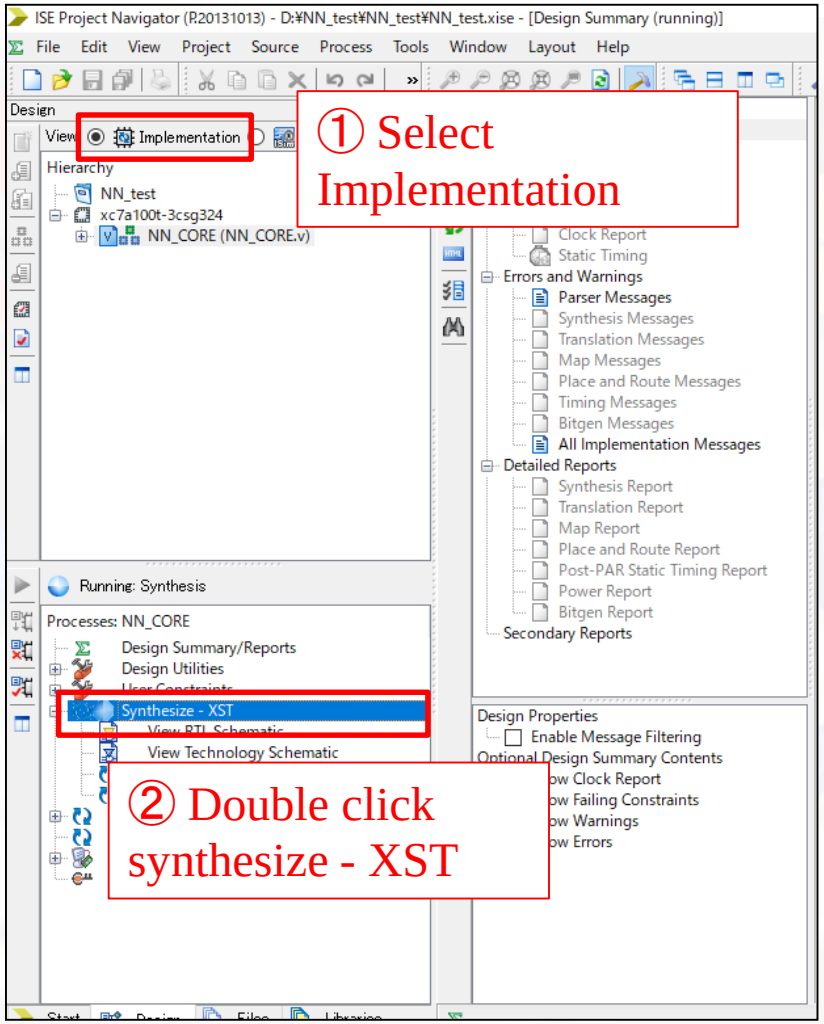




② Click OK

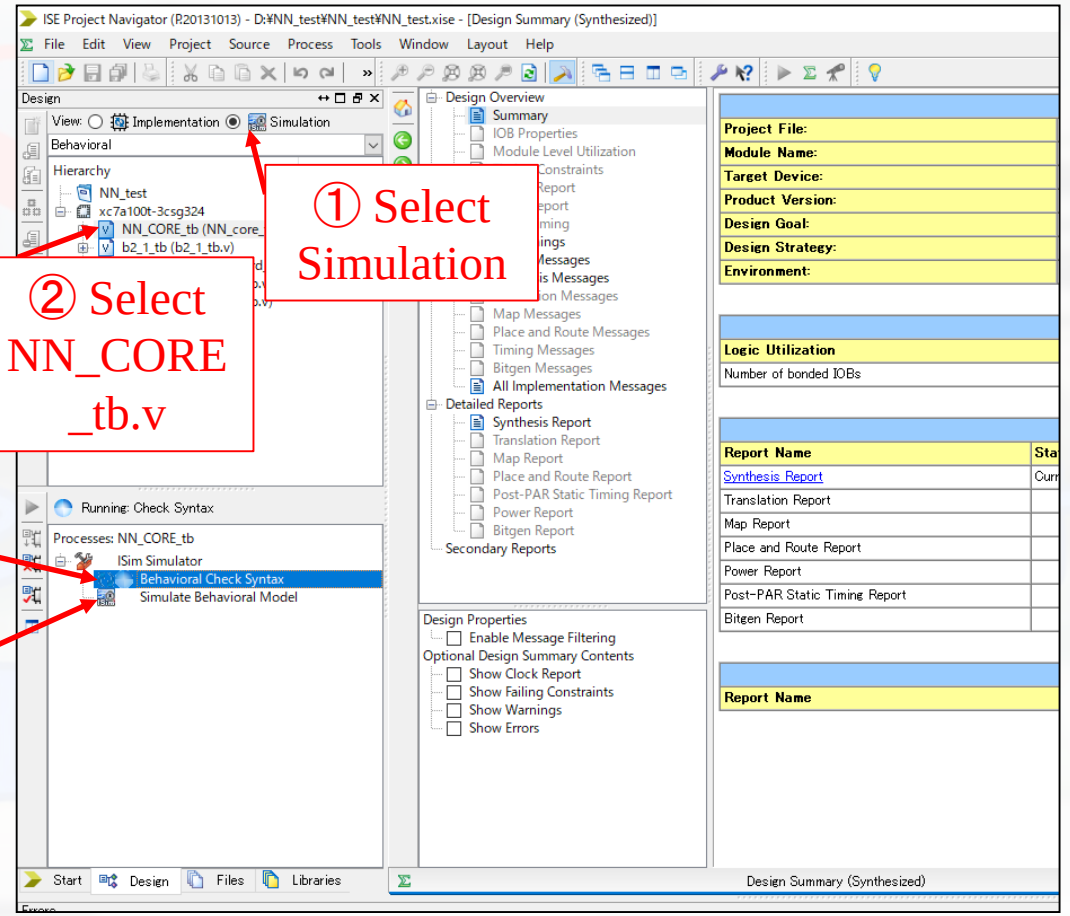
Synthesize the project

- Select Implementation
- Double click synthesize – XST
  - Wait until it finish



Simulate the project

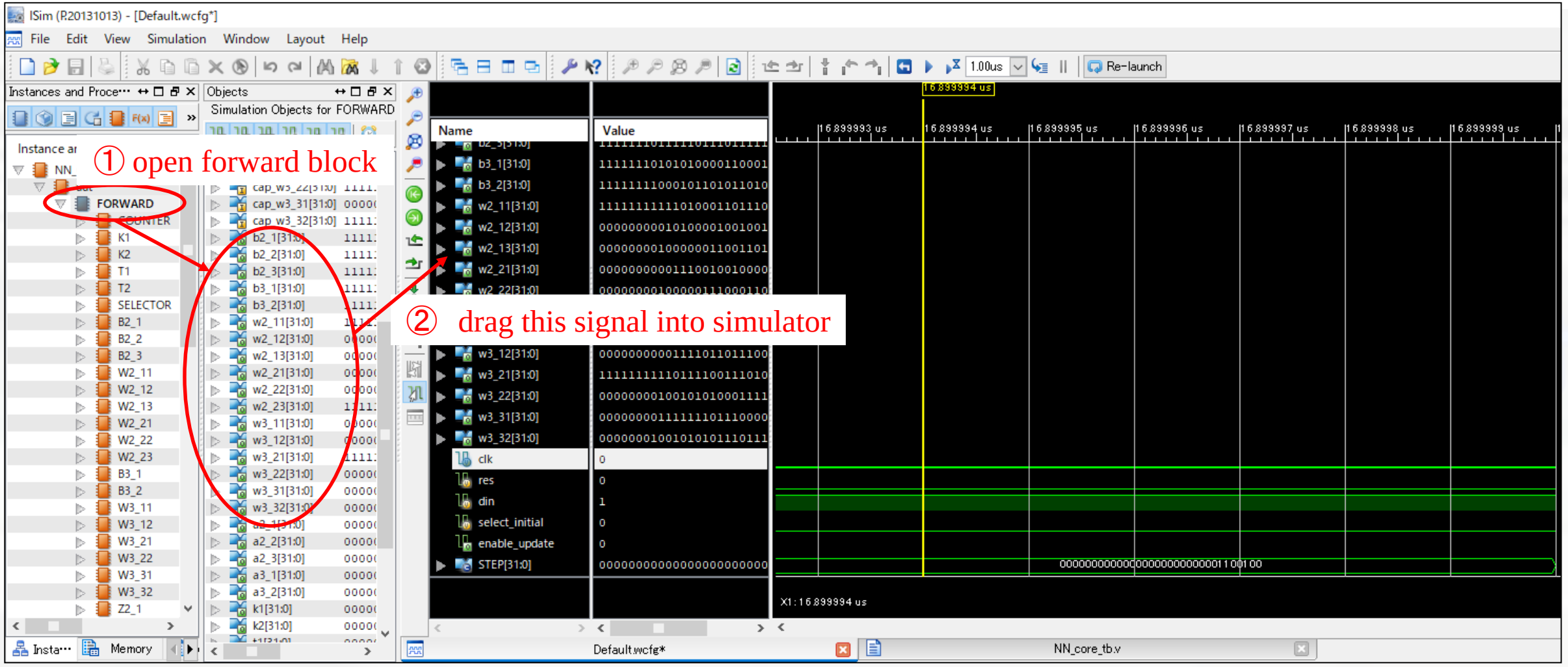
- Select Simulation
- Double Behavioral Check Syntax
  - Wait until it finish
- Double click Simulate Behavioral Model



ISE Simulator

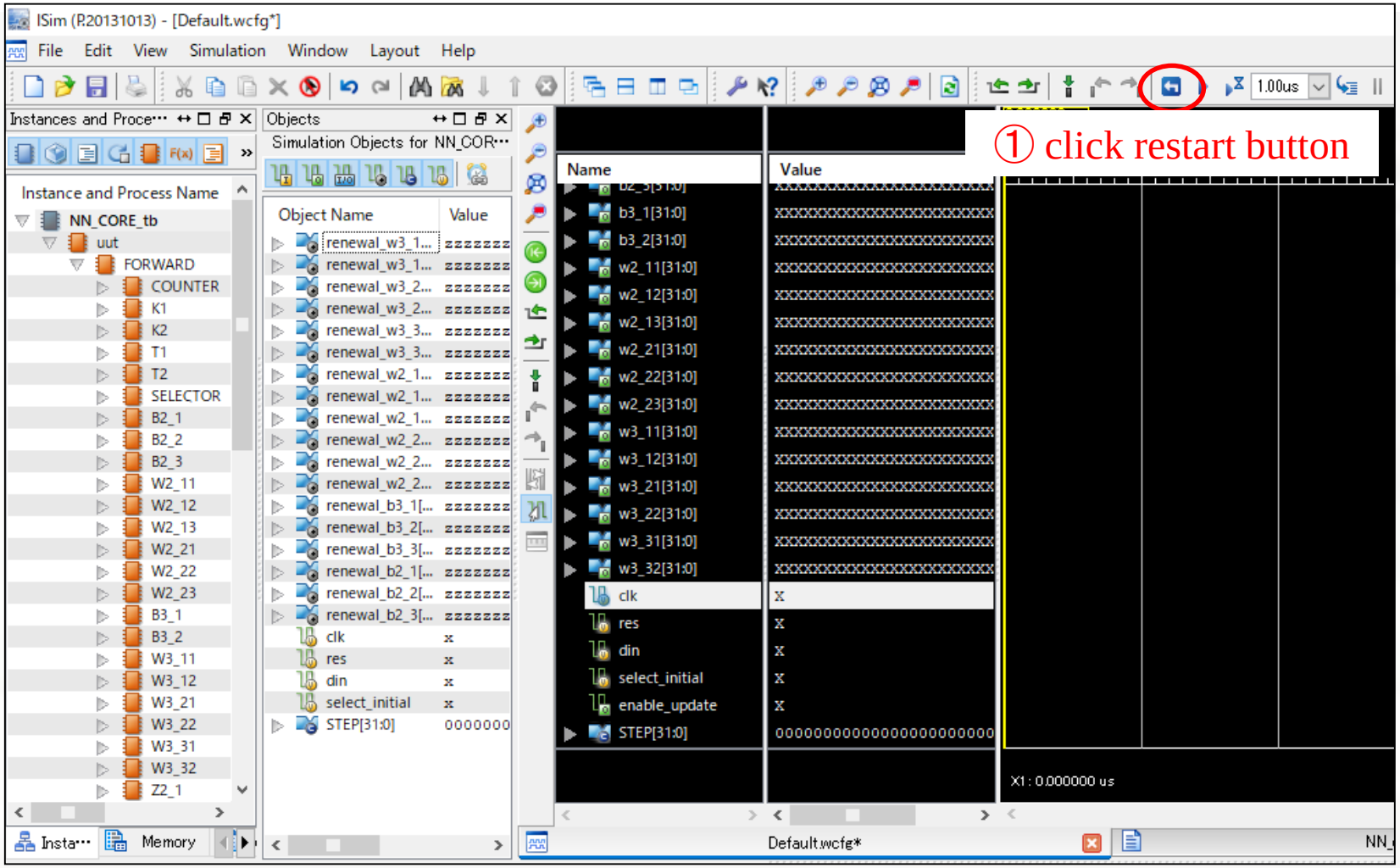
- ISE simulator will open
- Choose forward block in instance and process name
  - Choose signal b2_1 until w3_32
  - Drag the signal into simulator
- Choose forward > selector block in instance and process name
  - Choose signal enable update
  - Drag the signal into simulator
- See the figure in the next slide…

ISE Simulator



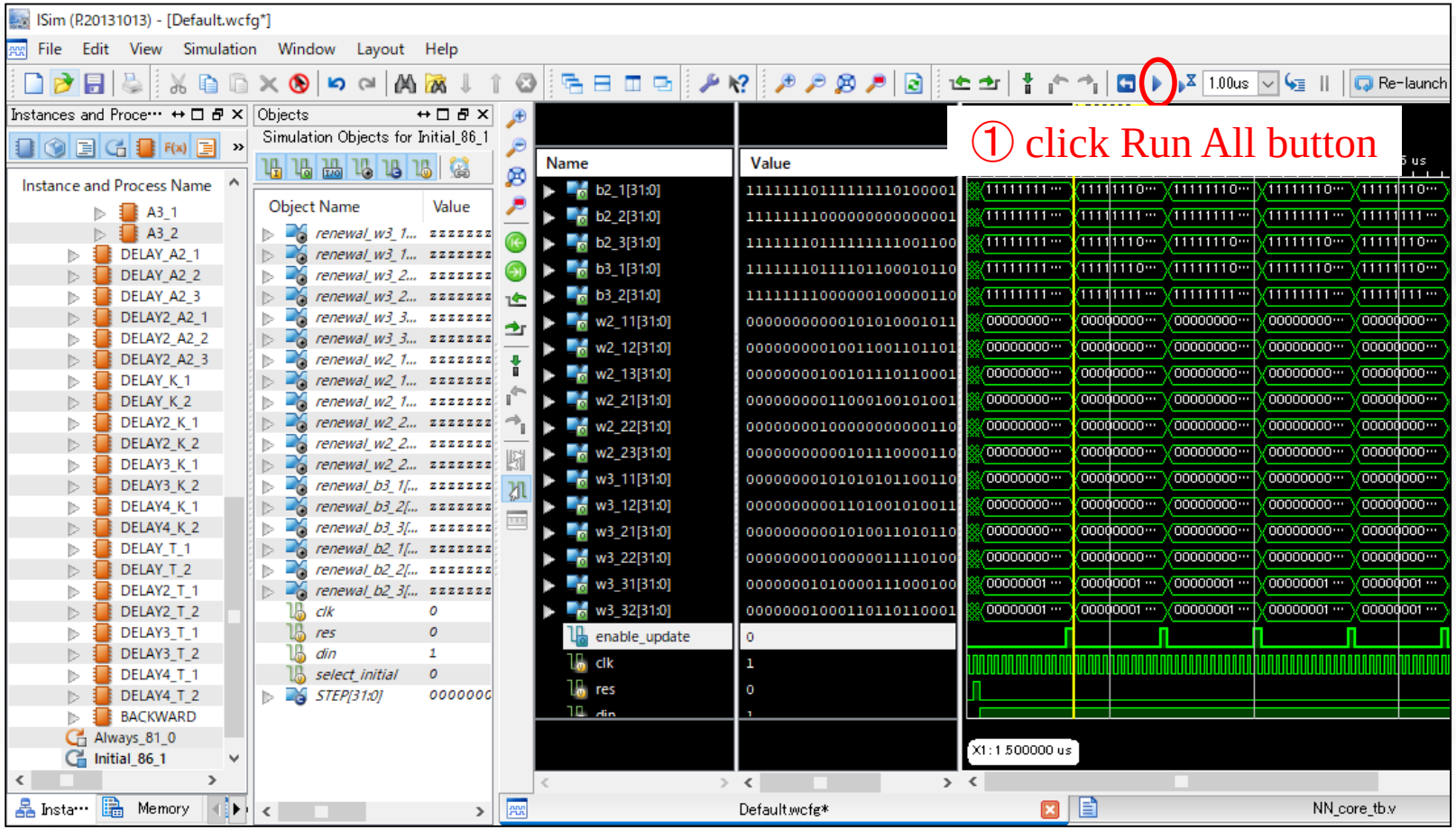
ISE Simulator

- Click the restart button



ISE Simulator

- Click the Run All button



Conclusion

- New weight and bias will be updated every time the enable update signal is active.
- In the current stage, the output does not converge.